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# Optimal of 1-bit Comparator design and Energy Estimation using Quantum Dot Cellular Automata

**V. Satyanarayana[1], M. Balaji[2], K. Neelima[3]**
[1]M. Tech Scholar, Department of ECE, Sree Vidyanikethan Engineering College, Tirupati-517102.
[2]Assistant Professor, Department of ECE, Sree Vidyanikethan Engineering College, Tirupati-517102.
[3]Assistant Professor, Department of ECE, Sree Vidyanikethan Engineering College, Tirupati-517102.

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**ABSTRACT**

Performance of CMOS technology has been affected in nanosystems due to power dissipation, area, and reliability functionalities. A research initiative which investigates other possible systems with related capacities is QCA. In this paper, QCA nanotechnology was used to create a 1-bit comparator. These circuits are easy to create and do not require any crossovers. The proposed design is extremely efficient in expressions of delay, cell count, area and quantum cost, which improves the performance within the range of 74.81% to 99.87% in terms of quantum cost. As a result, proposed designs are often found in various digital logics that require a small amount of space and low power consumption.



***Corresponding Author:***

V. Satyanarayana,
Sree Vidyanikethan Engineering College,
Tirupati-517507.
Email: satyab.tech4@gmail.com

## 1. INTRODUCTION

The reliability of efficient transistor Semiconductor devices has strengthened the driving force behind the semiconductor industry's accelerated growth, chip density, lower power dissipation, and faster integrated circuit switching speeds. The quantum effect is significant in the operation of transistors in the deep nanometer environment. Other aspects with deep nanometer transistor circuit architecture include high energy consumption, power losses, and electron leakage [1-3]. It includes present and prospective application of digital systems; developing nanotechnologies are an exciting investment opportunity [2, 5, 6]. QCA is a fast-evolving technology for computational logic designs as well as solutions to CMOS in nanosystem issues [4, 7]. Since QCA can be built using molecules, its scalability is much preferable than that of silicon-based transistor scaling for CMOS.

### A. QCA Nanotechnology

Nanotechnology based on QCA is one of the most efficient technologies being explored and researched by researchers. In 1993, C. S. Lend [1] was the first to suggest the concept of QCA. In order for the measurement and transformation process [4,7] the structure between cell charges is required and QCA is included in the cell concept. The elimination of cell contact wires or interconnection is another benefit of QCA electronic circuit design. There are four quantum dots or wells in each cell as shown in figure 1. In

this process, only two electrons are limited. Quantum tunnel junctions separate these quantum dots. The electron flow is caused by coulombic interaction between the cells. Electrons only arise at antipodal sites, ie. diagonally, due to coulombic repulsion, resulting in minimal repulsion. These electron residing positions eventually lead to the binary '0' and binary '1' polarisation states. The polarisation states of QCA cells are represented in Figure 2. In QCA [3, 8], energy dissipation is negligible during propagation and state transition, resulting in a low energy dissipation as compared to CMOS technology.

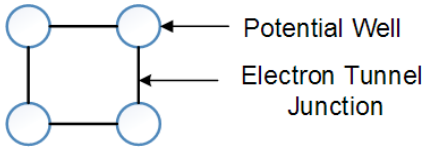


Figure 1. Schematic of QCA Cell.

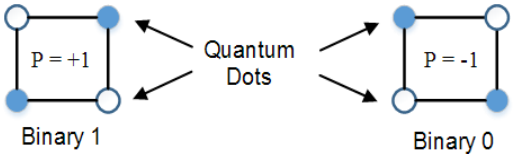


Figure 2. Binary QCA Cells.

### B. QCA in Clocking

In addition, QCA circuit has four phases, each of which has a 90 degree differential between the circuit and only two clocking states: 'LOW' and 'HIGH.' The quantum tunnelling of electrons to other points in an input phase of a clock at certain stages by raising or lowering the barrier potential. Pipelining is a phenomenon that allows data to be transmitted. Switch, release, relax, and hold are the four steps of this clocking. Since the QCA cells are unpolarized at first, they have a low potential.

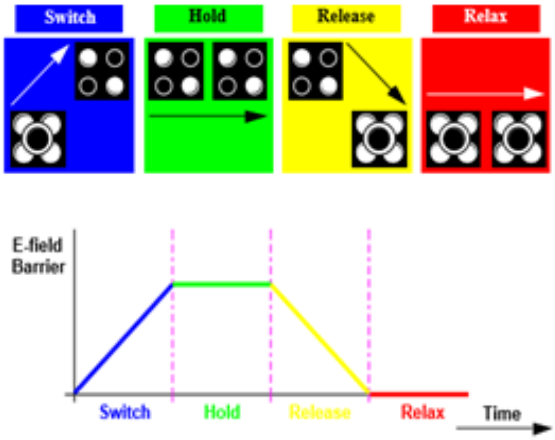


Figure 3. Different clock phases in QCA.

During the switch cycle, the polarisation of a QCA cell is largely determined by the polarisation of adjacent cells, and the potential vitality of the electrons rises exponentially. Furthermore, no state change happens when the electron exceeds its full potential viability at the end of the switch stage. Cells maintain their previous state throughout the keep process, and their potential viability remains high. The electrons potential energy continues to decrease during the release and relaxation phase, gradually leading to null polarisation [4, 6, 7]. Figure 3 shows different clock stages.

### C. QCA with Crossovers

In circuit design, QCA wires crossover is usually used for simpler designs. Two forms of crossovers have been found in QCA. They are coplanar and multilayer crossovers. To crossover the wires, coplanar crossover is carried out in a single plane using direct and rotated cells is as shown in fig. 4, since there is no interaction between the cells or the use of alternative clock zones for crossovers. The other is a multilayer crossover, as

shown in figure. 5, which has more than one layer. Although multilayer crossover is more difficult to design than coplanar crossover, it is preferred because it reduces the number of cells and circuit area [1]. However, coplanar is preferred in terms of fabrication possibility.

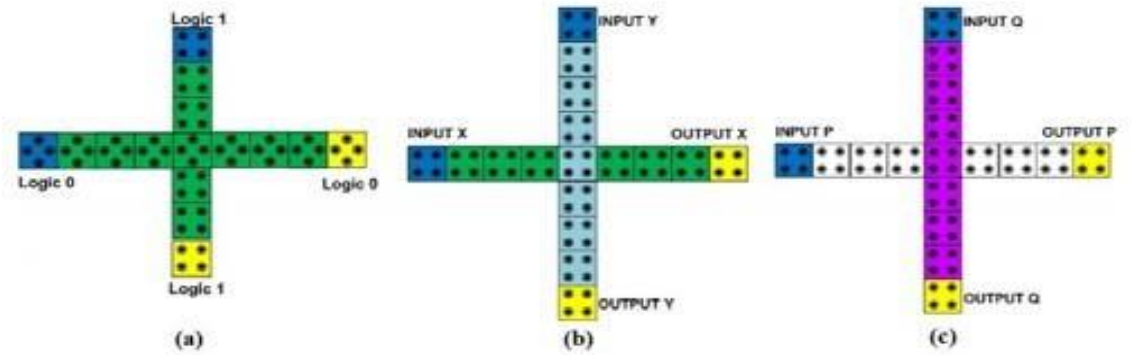


Figure 4. QCA crossovers (a) with rotated cells, (b) with clock0 and clock2, (c) with clock1 and clock3.

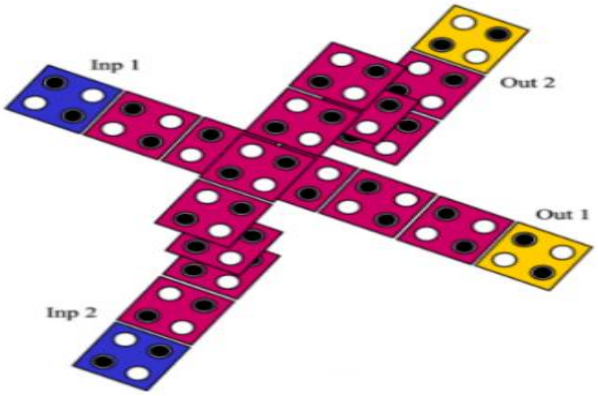


Figure 5. QCA with multilayer crossover.

## 2. 1-BIT COMPARATOR

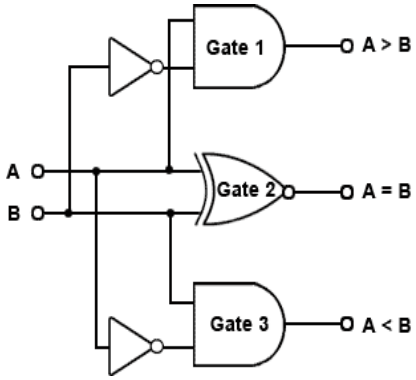


Figure 6. Logic diagram for a one-bit Comparator.

Binary comparators are used for optical comparators. Binary bits are measured by the 1-bit comparator to decide if one is greater and equal or less. Logic diagram of a one-bit comparator shows above.

$$Y1 = AB' \quad (1)$$

$$Y2 = AB + A'B' \quad (2)$$

$$Y3 = A'B \quad (3)$$

Here Y1, Y2 and Y3 are output equations. This one-bit comparator logic circuit appears in figure. 6 and the Truth Table is also shown in below.

Table I. Truthtable for 1-bit comparator.

| INPUT | | OUTPUT | | |
|---|---|---|---|---|
| A | B | Y1(A>B) | Y2(A=B) | Y3(A<B) |
| 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 |

**A. Literature Review**

To analysis the various 1-bit comparators proposed in QCA, a literature review was conducted. A few designs that have been proposed are seen below figures. Other architectures build the comparators with reversible gates[2-6], but they use a multilayer or rotating cell solution with a very high cell count[4]. The conceptual designs are configured with only majority gates, but this usually leads to use the more no. of fixed cells of polarization which is inefficient from a design technology [4,5]. Figure 8 hires 87 cells to play the role of a 1-bit comparator. Figure 9 shows a multilayer architecture with fewer fixed polarization cells to achieve the desired goal with cell count of 73 cells and less number of cells. Many researchers implemented QCA comparator circuits earlier. In Ref[1] a coplanar QCA Comparator Circuit with 0.182 μm2 and 117 cells was constructed, as shown in Figure.7. A single-bit comparator was proposed in Ref. [2]. A multi-component structure with a 0.11μm2 and 87 QCA cells as shown in figure.8 will be required for this QCA comparator circuit. In Ref[3] a multi-layered QCA Comparator Circuit with 0.06 μm2 and 73 cells was constructed, as shown in figure.9.

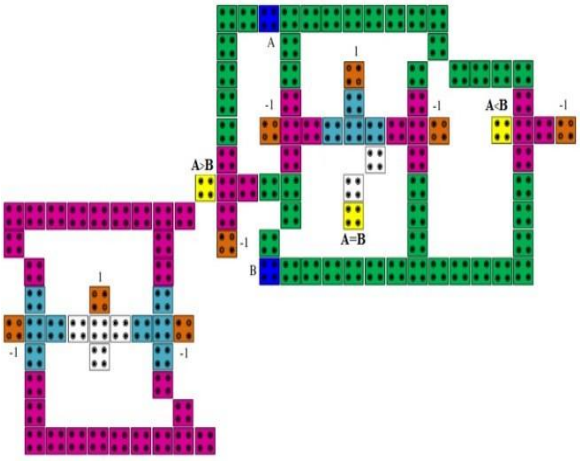


Figure 7. 1-bit Comparator with 117 cells.

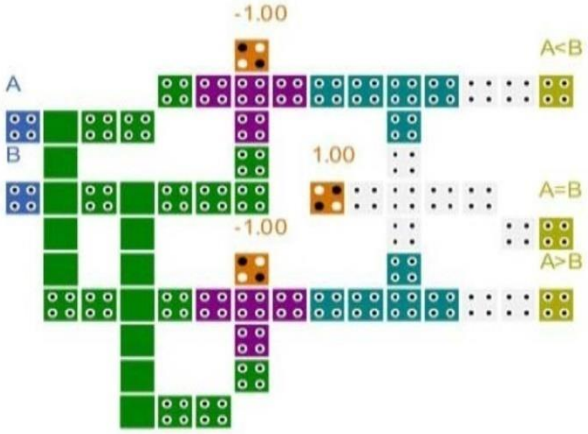

Figure 8. 1-bit Comparator with 87 cells.

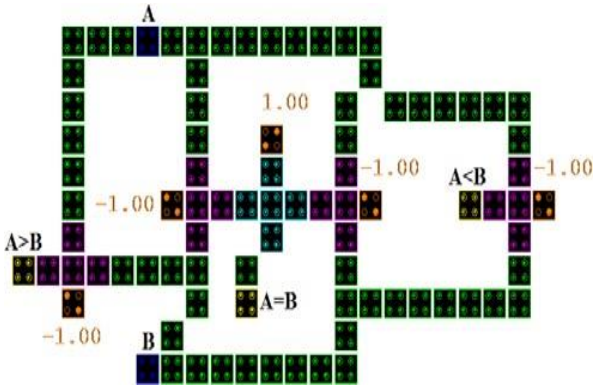


Figure 9. 1-bit Comparator with 73 cells.

**B. Existing Design**

A few 1-bit comparator designs are shown in figures 10,11, but the majority of these have a large area of cells and cell count. Various concept crossovers are also used in these designs. Moreover, the circuits latency is higher, leading to a higher quantum cost. Figure 10 shows a one-bit comparator with no crossover based on these conditions. The simulation results from the QCA Designer 2.0.3 tool, as seen in figure.12, can be used to check the design's effectiveness.

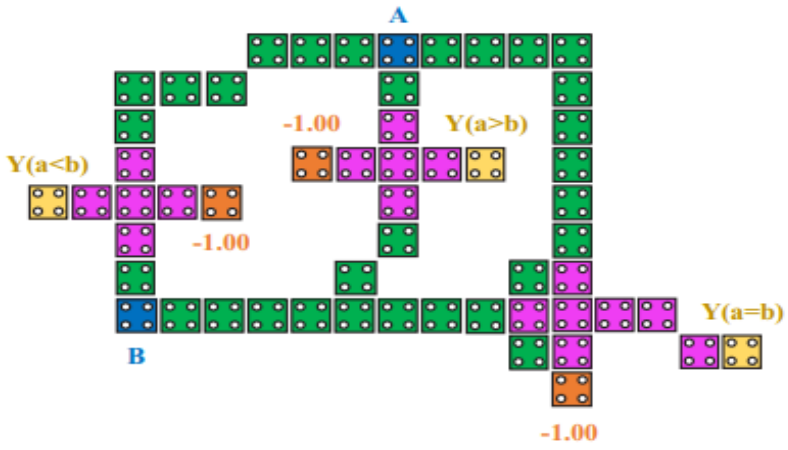


Figure 10. QCA Schematic Design-1 for 1-bit Comparator with 55 cells.

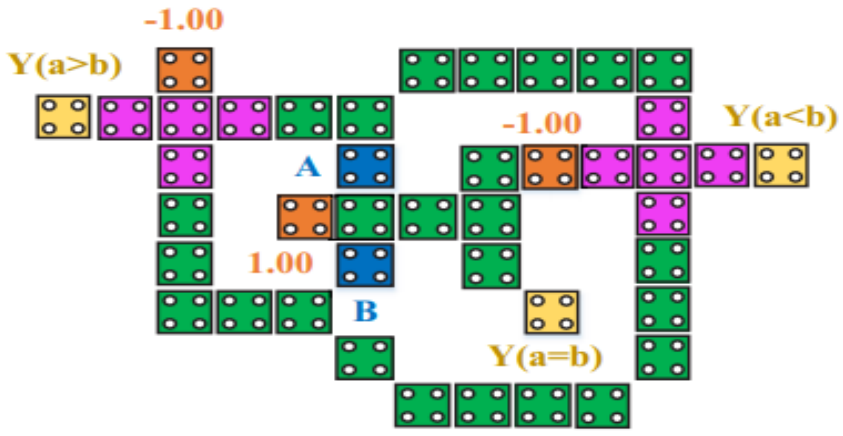


Figure 11. QCA Schematic Design-2 for 1-bit Comparator with 42 cells.

There are 55 cells in the design, with a total area of cell is 0.0669 μm2. The XOR gate, which has only 42 cells and area of cell is 0.0407 μm2, was optimised to produce another architecture, as seen in fig. 10.

### C. Proposed Design

The 1-bitcomparator design in fig.10 has a large cell area and cell count. In addition, the circuits' latency is higher, resulting in a higher quantum cost. This paper proposes a new 1-bit comparator without using crossovers as seen in fig.12. The simulation results from the QCA Creator v2.0.3 tool can be used to verify design's accuracy, as seen in figure.13.

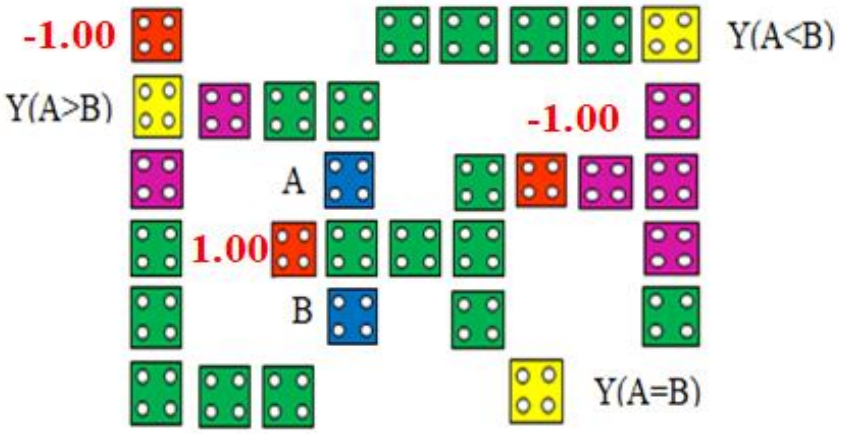


Figure 12. QCA Schematic for 31 cells 1-bit Comparator.

The proposed schematic design has 31cells with the total area of cell is 0.03μm$^2$.

### D. Comparison table

| Design | Cell Count | Total Area (μm$^2$) | Delay (clock cycle) | Crossover | Quantum Cost |
|---|---|---|---|---|---|
| [1] | 117 | 0.18 | 1 | Coplanar | 0.0275 |
| [2] | 87 | 0.11 | 0.5 | Coplanar | 0.0275 |
| [3] | 73 | 0.06 | 1 | Multilayer | 0.06 |
| Existing Design-1 | 55 | 0.06 | 0.5 | Nil | 0.0167 |
| Existing Design-2 | 42 | 0.04 | 0.5 | Nil | 0.0102 |
| Proposed Design | 31 | 0.03 | 0.5 | Nil | 0.01 |

### E. ENERGY CALCULATION USING QDE

If qca cells are separated for each clock cycle, they form a "bath" of energy, as described in qde. ebath is the total amount of energy transmitted to the qca'bath.' As a result, the sum of all ebath energies will be used to calculate total energy dissipation. The 3 main components of energy dissipation are eck, eev, and eio. eck is used to transfer energy to clocks, eev is used to transfer energy to the atmosphere, and eio is used to transfer energy to neighbouringqca cells. It's worth noting that ebath = eev, and this is a contradiction. The equation is eio = eout, where ein is the amount of energy entering the cell and eout is the amount of energy exiting the cell.There may be an error in the measurement of electricity, which can be expressed as err = eev(eck + eio). If the error is negative, the energy has been converted from the three components previously discussed. Average loop energy dissipation is 1.50e-003e ev, with minute error -1.48e-004e, while the 1.65e-002e-bit comparators are used with a negligible error of -1.63e-003ee ev and with total energy. The qde tool was used to calculate the energy dissipation of each coordinate.

| Design | Total Energy Dissipation | Average Leakage Energy Dissipation |
|---|---|---|
| [1] | 0.3808 | $-4.02*10^{-3}$ |
| [2] | 0.182 | $-3.59*10^{-3}$ |
| [3] | 0.106 | $-3.05*10^{-3}$ |
| Existing Design-1 | 0.095 | $-2.93*10^{-3}$ |
| Existing Design-2 | 0.0603 | $-1.66*10^{-3}$ |
| Proposed Design | 0.016 | $-1.63*10^{-3}$ |

## 3. RESULT

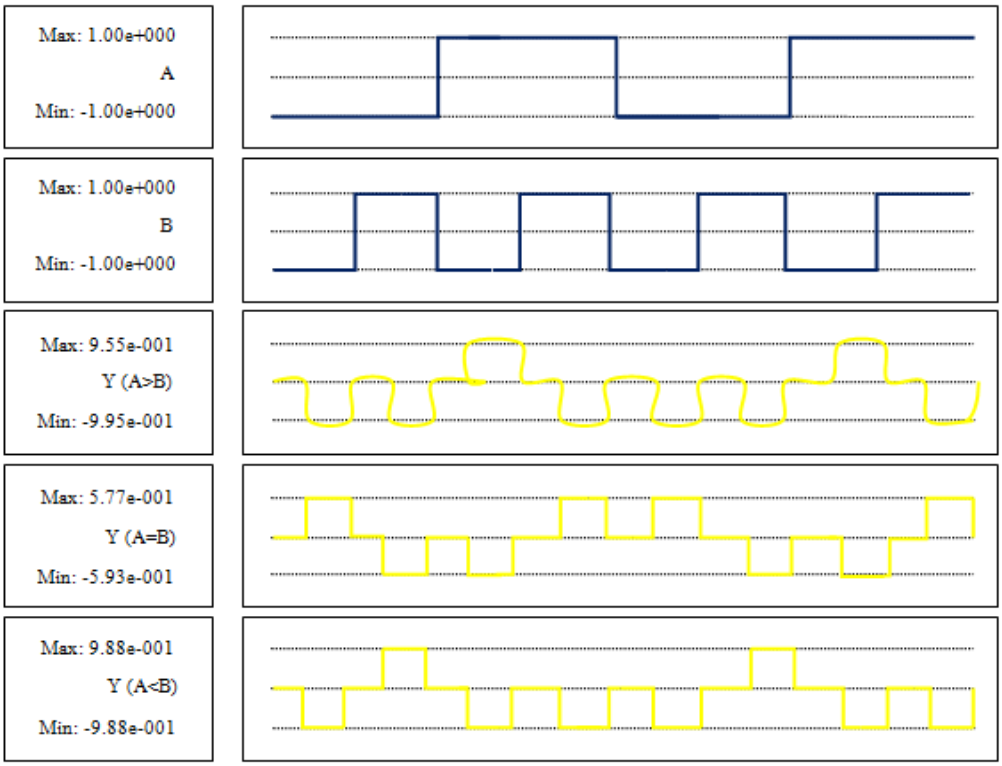


Figure 13. Waveform simulation for the QCA 1-bit comparator

## 4. CONCLUSION

According to the result the comparator design is proficient in terms of delay, area, quantum cost, cell count andit achieves performance of 72.91% to 99.87% over current proposed design, there are many designs to consider in expressions of quantum cost. As a result, the proposed design is used in a variety of technology with negligible space and low power consumption.

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## BIOGRAPHIES OF AUTHORS


| | |
|---|---|
|  | V. Satyanarayana<br>M.Tech Scholar, Department of ECE,<br>Sree Vidyanikethan Engineering College, Tirupati – 517102<br>satyab.tech4@gmail.com |
| | |
|  | M. Balaji<br>Assistant Professor, Department of ECE,<br>Sree Vidyanikethan Engineering College, Tirupati – 517102<br>balajichaitra3@gmail.com |
| | |
| | K. Neelima<br>Assistant Professor, Department of ECE,<br>Sree Vidyanikethan Engineering College, Tirupati – 517102<br>neelumtech17@gmail.com |